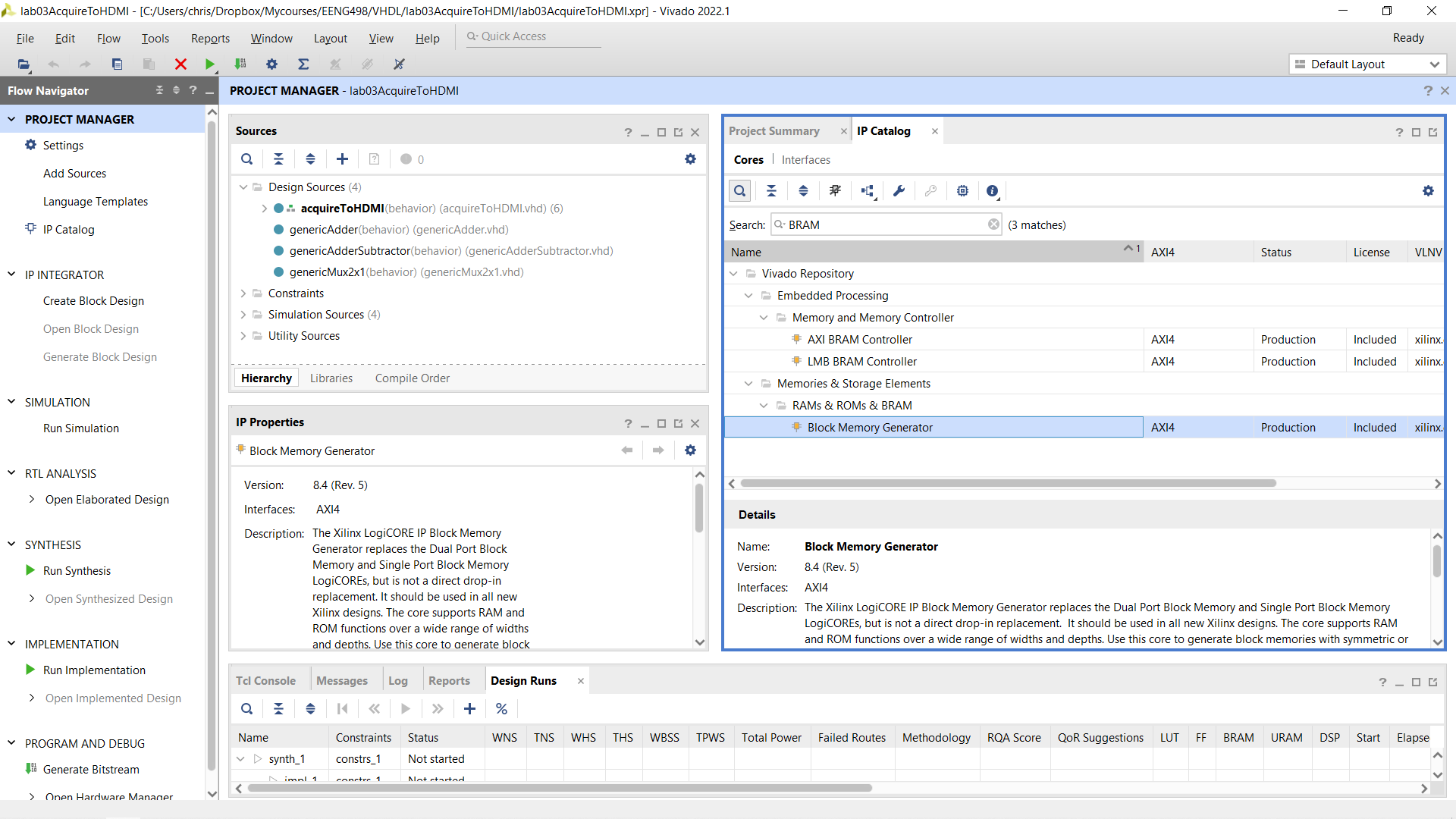
The Zynq7000 chip comes with a lot of built in hardware. This specialized hardware is called Intellectual Property or (IP). You can access the Xilinx IP for the Zynq using the following process – we will only use it for block RAMs, but there are other options in there and I invite you to look around.

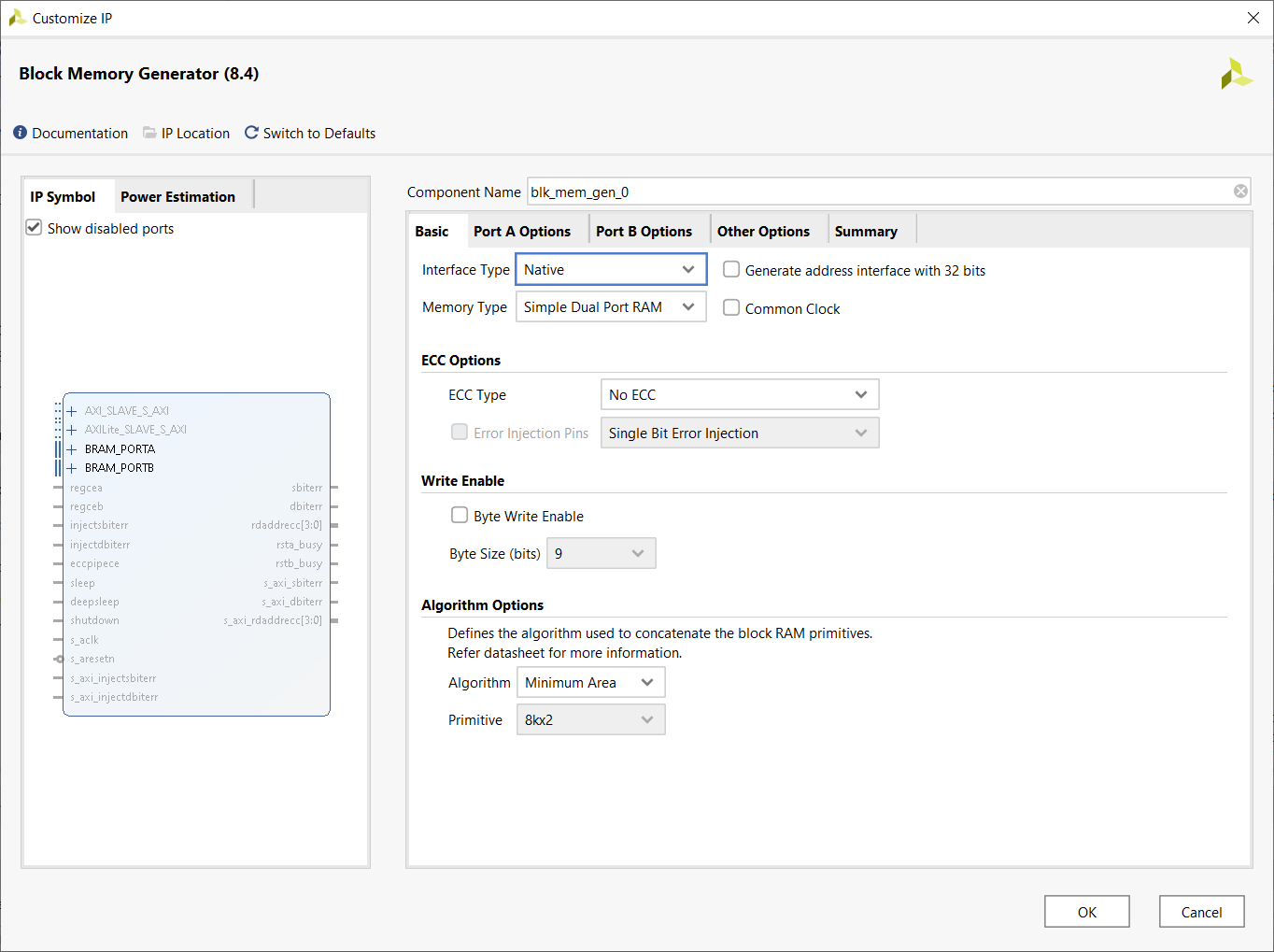
You will need block RAM to store sampled data so that the scopeFace component can display it on the oscilloscope. Reating the block RAM is straightforward using the following steps. Start by opening the IP catalog using the link in the Project Manager area on the left of the screen.

Search for BRAM in the IP Catalog tab. Click on the Block Memory Generator line.

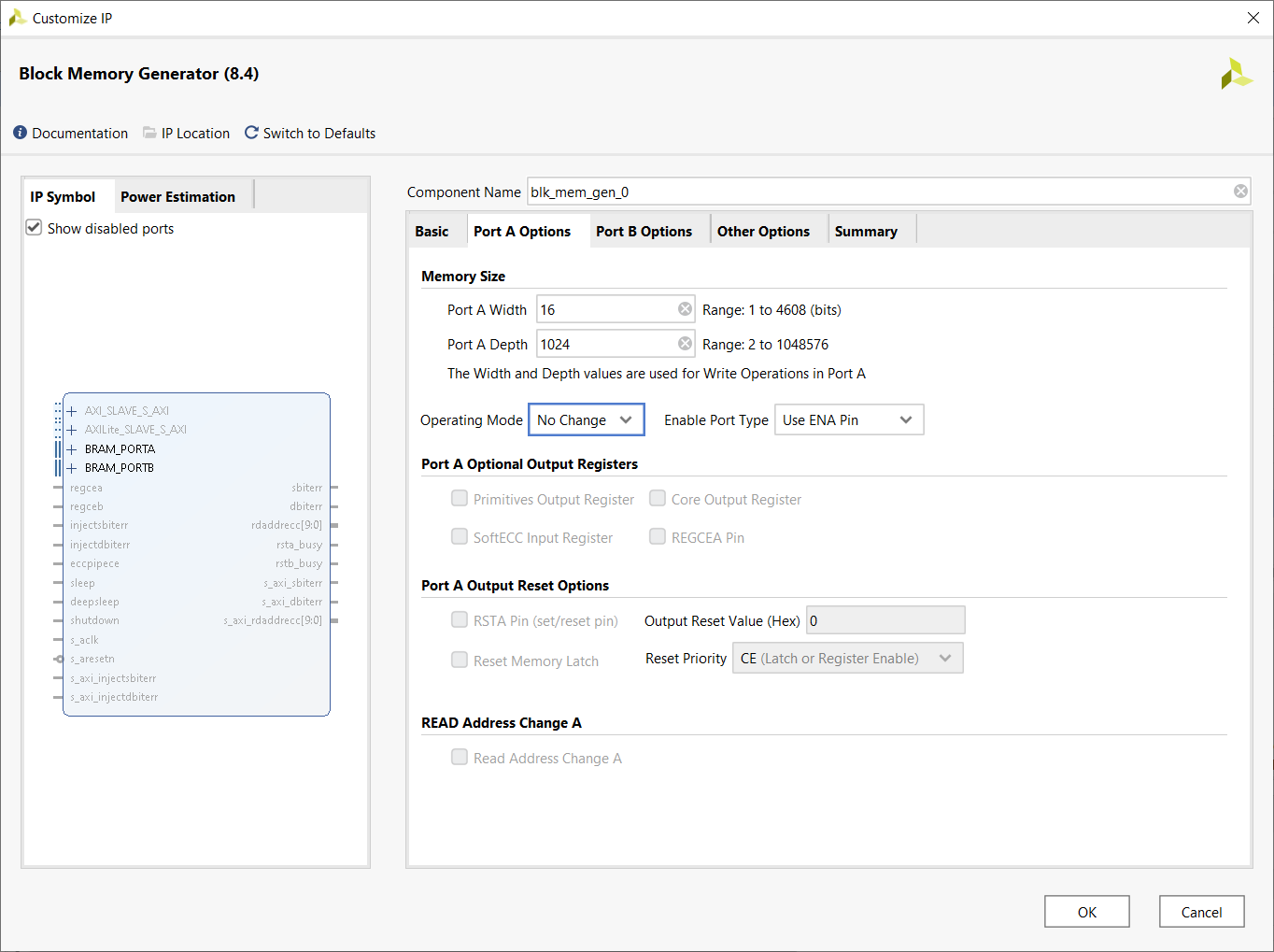


To configure the Ram, step through the tabs at the top of Customize IP pop-up.

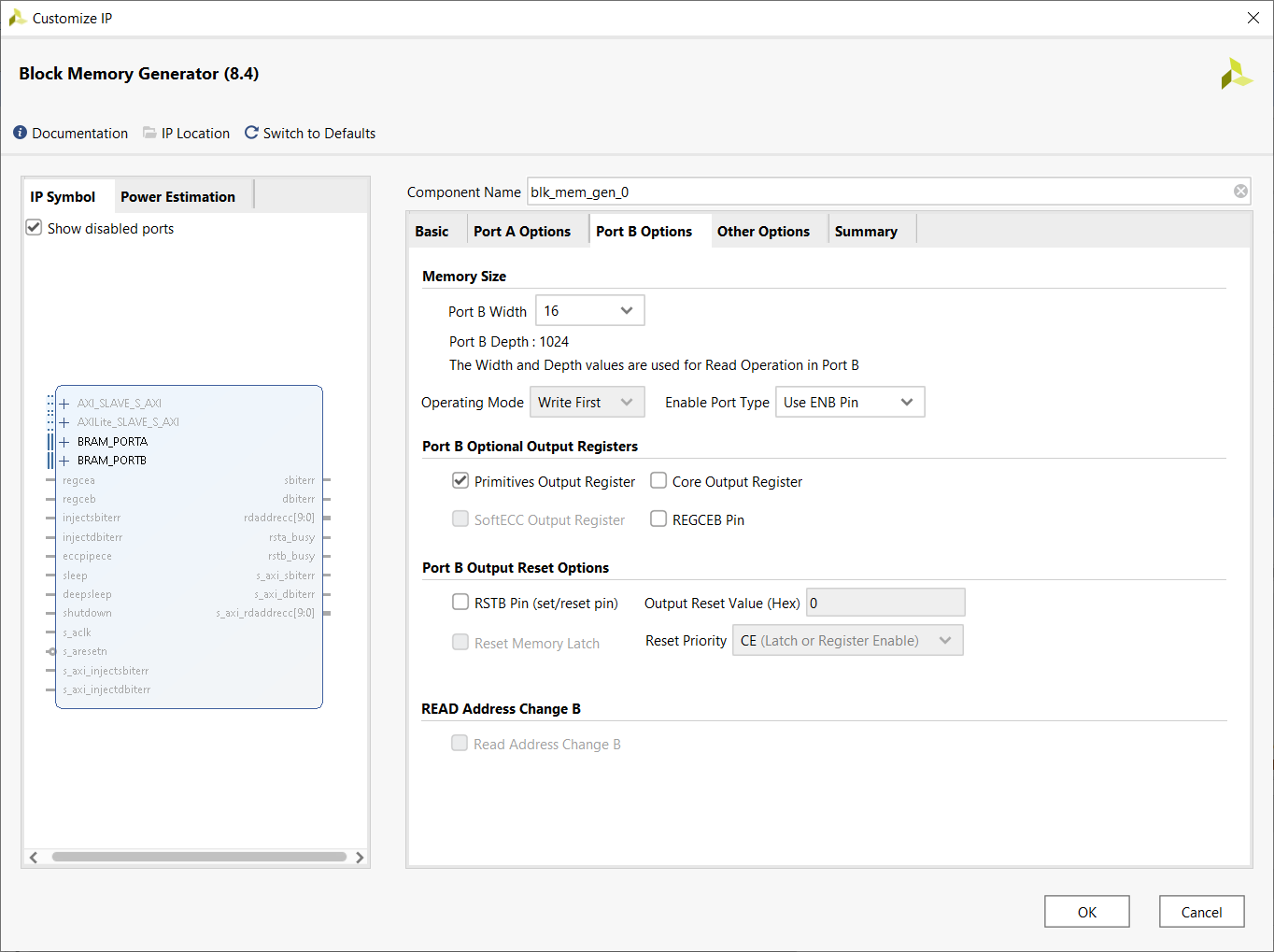
**Basic**: Select Simple Dual Port RAM



**Port A:**  Change the Port A depth to 1024 and set any options shown below.



**Port B:** Set any options shown below.



**Other Options**: Leave the defaults alone

Click OK to complete adding this memory to your design. You can instantiate this memory as many times as needed.

Since you will have to interface to the block RAM, you will need to put its component declaration in your package file. To get the entity definition of the block memory:

* Go to Sources in the Project Manager area and expand the blk\_mem\_gen\_0 unit
* Double click on the blk\_mem\_gen\_0\_arch
* The entity will show up in the text editing area

